Process and environmental variations are becoming a more significant problem in integrated circuit design as devices continually get smaller. Circuit designers must take these realities into account to ensure that their devices function correctly. Process variation is typically broken into two categories: die-to-die variation (D2D) and within-die variation (WID).

Temporal variations in Vdd and temperature are included in the category of environmental variation. Negative Bias Temperature Instability is another temporal variation that causes the threshold voltage of PMOS devices to degrade over time. Over time, a negative bias on the device generates interface traps at the Si/SiO2 interface, which in turn causes a shift in the threshold voltage of the device. This can significantly reduce the speed of a circuit and reduce its overall lifetime.

Most of the implantable on-chip variation sensors that have been developed only quantify the global variation factor using a simple ring oscillator circuit. This is because the frequency dependency of ring oscillators on process and environmental variations provides a convenient way to quantify these variations on a chip. Ring oscillators can be used as a sensor embedded in a chip to measure temperature and prevent it from negatively affecting the circuit functionality. By making some changes in the oscillator structure, variation impacts on individual transistors can be observed. Our main motivation is to measure the changes in the circuit functionality due to temperature fluctuations, supply voltage noise sensitivity and process variations. Corner analysis and Monte Carlo simulations will need to be performed in order to see how process variations and temperature change affect the degradation of circuit performance.

The Agarwal paper [5] we read employs a novel circuit that can actually quantify the local and global variation on a chip. This circuit provides the ability to select single FETs to provide a virtual Vdd or Gnd for the ring oscillator. By rotating through various FETs and measuring how the frequency varies with each device, the variation of each device in relation to each other can be determined. We plan to develop a 1st-order Verilog-A transistor model of a PMOS device that takes the NBTI-induced threshold voltage shift into account. Simulating the Agarwal circuit using this device we will be able to directly link the ring-oscillator frequency with the degradation of the PMOS device. For our project we plan to expand on the Agarwal circuit to be able to quantify the effects of process and environmental variation factors.

In order to verify the functionality of the Agarwal circuit, we built a replica in Cadence. We began by developing the mux, latch, and flip-flop components (Figures 1-4). Next, we put the pieces together to create the complete circuit (Figure 5). Initially, the ring oscillator was not oscillating properly (Figure 6). We traced the problem back to an issue with our mux design, fixed the problem, and continued testing. We then ran the circuit with one PMOS on and measured the value of the virtual Vdd and the ring oscillator’s frequency (Figures 7-8). We did the same test with only 1 NMOS on and also with 6PMOS’s and 5NMOS’s on (Figures 9-11). As we expected, the frequency was highest when half the devices were on and half were off (providing both a strong Vdd and Gnd). All of these simulations were performed at the default temperature, 27°C.

We then did the same test again, but varied the temperatures from 30°C to 120°C. These outputs are seen in Figure 12-13. The results are plotted in Figure 14. Again, as expected, higher temperatures result in lower oscillating frequencies.

We attempted to develop a plot of oscillation frequency for varying values of Vdd, but we came across problems implementing the simulation. We had also hoped to have run a Monte Carlo simulation at this point, but we did not figure out how exactly to accomplish this yet. Joe Ryan’s tutorial on Thursday will hopefully provide us with the knowledge to accomplish this goal. These two simulations will be the next steps in our project. We also plan to alter the Agarwal circuit to add the ability to provide increased negative bias on individual PMOS devices to increase the speed of the Vt degradation due to NBTI. Developing the Verilog-A transistor model will be another important milestone for our project to reach.

Another essential part of this project will be to maximize the sensitivity of the oscillator frequency to the parameters of the surrounding FET devices. We will have to figure out the perfect sizing ratios to ensure that the variations in the oscillating frequency are primarily due to the devices that we are testing and not on other outside factors.